

May 17, 09 14:42

pcb\_turnon\_notes.txt

Page 1/5

```

1 #*****
2 #
3 # turnon_notes.txt module
4 #
5 #*****
6 #
7 # VCL Confidential Copyright © 2009 UC Davis, ECE Department
8 #
9 #*****
10 #
11 # created on:    04/28/2009
12 # created by:   jwwebb
13 # last edit on: $DateTime: $
14 # last edit by: $Author: $
15 # revision:     $Revision: $
16 # comments:     Generated.
17 #
18 # board name:      MSEE Thesis Measurement Board
19 # board number:   P342
20 # board revision: 001
21 #
22 #*****
23
24 #-----
25 # T U R N O N N O T E S :
26 #-----
27 1. No shorts on power supplies.
28     - Board Powers Up Properly.
29     - All supplies within spec.
30 2. Control FPGA Programs via JTAG successfully.
31     - Using Xilinx IMPACT Software.
32 3. SPI Configuration PROM programs via JTAG successfully.
33     - Using Xilinx IMPACT Software.
34 4. Data Path FPGA Programs via JTAG successfully.
35     - Using Xilinx IMPACT Software.
36     - Operates at about 42 degrees C with Fan Sink.
37     - Operates at about 62 degrees C without Heat Sink.
38 5. Control FPGA RS-232 (CP2102) interfaces functions correctly.
39     - Operates a 115.2kBaud
40     - Read/Write control of Control FPGA registers.
41 6. Control FPGA controls Data Path FPGA successfully via "ilb_master".
42     - LEDs turn on and off.
43     - Block RAM read registers respond correctly.
44 7. 1GHz VCO operating correctly.
45 8. 10MHz Internal/External circuits operating correctly.
46 9. 100MHz LVDS oscillator on both the Control FPGA and Data Path FPGA
47    operating correctly.
48 10. Power CPLD Programs via JTAG Successfully.
49 11. Power CPLD receives 10MHz and properly distributes 312.5kHz
50     to all DC-DC Converters.
51 12. Attempted to configure AD9516 Clock Generator
52     - Verilog HDL Driver verified in simulation.
53     - Doesn't seem to be configured properly.
54     - Double-check config registers to verify VCO is turned on properly.
55     - It turns out there were a couple of problems.
56     a. The SPI interface wasn't working very well at all. For example,
57        I meant to write data 0x99 to address 0x000, but it was writing
58        0x20 to address 0x013. For some reason the data was shifted to
59        the left by 5 bits. I simulated the design & it looked correct,
60        so I just played around with the SCLK and SDIN shift registers.
61        Eventually I was able to get it to look correct and I could
62        read/write data reliably with a Perl Script.

```

May 17, 09 14:42

pcb\_turnon\_notes.txt

Page 2/5

```

63         b. Once the SPI was fixed I could see clocks on all the desired
64           outputs, but the frequencies were all off. I had set the
65           Divider Low/High Cycles to 1 each for a divide by 2, but
66           it was actually dividing by 4. I set them both to 0, and I
67           got 500MHz out of my LVPECL outputs. The LVDS outputs were
68           really off, because there are two dividers in that path.
69           Now I'm getting the correct frequencies on all paths.
70         - I still need to tweak the differential voltages to get the correct
71           common mode voltages. Some of them aren't where they should be.
72 13. Attempted to configure DAC5682Z 16-bit DAC.
73     - Verilog HDL Driver verified in simulation.
74     - Add read capability in hdl driver to verify functionality.
75       a. See item 14.
76 14. Ported over MicroBlaze design from work project and verified that the
77     DDR SDRAM is working correctly.
78     - Bootloader Application successfully read out the MicroBlaze
79       application from the SPI Configuration PROM and transferred the data
80       to the DDR SDRAM.
81       a. The Bootloader then successfully jumped to the application
82         address 0x8c000000 and the MicroBlaze application began
83         executing out of the DDR SDRAM.
84     - The MicroBlaze application successfully read the DPIMAGE.bin file
85       from the microSD card and configured the Data Path FPGA via
86       a serial interface.
87       a. The Data Path FPGA successfully programmed.
88       b. The microSD card functions properly.
89     - The MicroBlaze application successfully communicates with the
90       Data Path FPGA via the ILB serial interface.
91     - The MicroBlaze application successfully transferred a waveform
92       from the microSD card to the Data Path FPGA.
93     - For some reason the I2C Fan Controllers don't seem to be working.
94       a. I get error messages pertaining to the iicWriteRegister.
95         i. This error was due to an incorrect I2C address.
96           The application was addressing Fan #1 at address 0x4C,
97           when it was really at address 0x18. Once the application
98           was updated the Fan Controllers started working properly.
99       b. Have some fans made up with connectors for testing the
100        fan controllers.
101     - AD9516 doesn't seem to be working with MicroBlaze application.
102       a. Probe Serial Data and Clock to see if data is being
103         transmitted at power-up.
104         i. For some reason my custom Verilog HDL Peripheral wasn't
105           shifting out 24 clocks, so the AD9516 wouldn't
106           properly configure. I adjusted the shift count clock, and
107           added a ChipScope Pro core to verify. I also discovered
108           that the read wasn't shifting in the last bit, so I
109           modified the shift register to clock read data in
110           on the positive edge of sclk. Now the AD9516 is properly
111           configured.
112       b. Create a debug command to configure AD9516 upon command.
113         i. Completed. See command 30.
114       c. Create a debug command to read AD9516 register.
115         i. Completed. See command 29.
116       d. Create a debug command to write AD9516 register.
117         i. Completed. See command 28.
118     - Add DAC5682Z peripheral configuration and control to current
119       MicroBlaze application and system.mhs/mss files.
120       a. Wrote SPI EDK Peripheral to control DAC5682Z via SPI Interface.
121       b. Initialization routine successfully completes.
122       c. Read/Write access correctly read/write to various registers.
123       d. Debug Commands:
124         i. Command 31: write command.

```

May 17, 09 14:42

pcb\_turnon\_notes.txt

Page 3/5

125           ii. Command 32: read command.  
126           iii. Command 33: initialization command.  
127       - Use ChipScope Pro to verify SRAM and Block RAM pattern  
128       playback inside of Data Path FPGA.  
129           a. Block RAM Patterns Play back successfully in ChipScope Pro.  
130           b. QDR-II SRAM Patterns Play back successfully in ChipScope Pro.  
131       - The 6 temperature sensors appear to be functioning properly.  
132           a. Temp: 30.5 C, 27.75 C, 26.75 C, 29.25 C, 28.25 C, 29.50 C  
133 15. DAC5682Z High-Speed 16-bit DAC Data Path.  
134       - Using MicroBlaze application I could configure the DAC5682Z via  
135       SPI; however, I couldn't see any data coming out of the Channel B  
136       DAC output.  
137           a. I read through my configuration settings and looked at the  
138       data sheet and discovered that my configuration settings  
139       were putting Channel B to sleep and the DAC in single-dac mode.  
140       Since my Anti-Image filter was being driven by Channel B,  
141       this explained why I wasn't seeing any data on the output.  
142       In probing the termination resistor on Channel A I was able  
143       to see data toggling. By setting the DAC5682Z to Dual DAC mode  
144       I was able to see data coming out of Channel B, but it was  
145       effectively decimated by 2. This was due to my FPGA design  
146       which was supposed to drive 8 consecutive packets of 16-bit  
147       data into the DAC rather than every other 16-bit packet of  
148       a 128-bit word out to Channel A. The DAC digital interface  
149       DDR, so it uses the 16-bit packet clocked in on the rising edge  
150       of DCLK for Channel A and the 16-bit packet clocked in on the  
151       falling edge of DCLK for Channel B.  
152           b. After reading the data sheet I discovered that when using  
153       the DAC5682Z in single-dac mode Channel A is the output.  
154       When I originally designed the schematics I was using  
155       Channel A, but during layout I changed to Channel B for  
156       layout reasons. Using Channel B meant I did not have to  
157       use vias in my analog signal path at the DAC output.  
158       Fortunately I chose to terminate the unused Channel A  
159       and used series 0 ohm resistors on the Channel B output  
160       before the Anti-Image filter. I forgot about the note  
161       in the data sheet regarding Channel A. The following PCB  
162       mod/butch was made:  
163           i. Remove R88, R89, R530, and R531.  
164           ii. Solder a wire from pad 1 of R88 to pad 2 of R531.  
165           iii. Solder a wire from pad 1 of R89 to pad 2 of R530.  
166       This mod/butch effectively changes the DAC output from  
167       Channel B to Channel A. The wire length is approximately  
168       3/4" long, so this shouldn't have a huge impact on the  
169       performance of my Signal Output because I'm only trying  
170       to generate signals from DC to 120MHz. If I were trying  
171       to generate signals at the full rate of the DAC, then  
172       I might be in trouble due to signal integrity effects.  
173       - After the PCB mod/butch was made, I was able to drive data  
174       out of the DAC5682Z. I could load various patterns into  
175       either Block RAM or QDR-II SRAM and play them back to the  
176       DAC5682Z. I was able to use the DAC Sync pin to turn the  
177       DAC5682Z output on or off.  
178       - The Signal Output waveforms driven from the OPA695 don't  
179       look too good. There's a lot of jitter and the noise floor  
180       is about -40dB. I expected the noise floor to be down  
181       at -60dB. I need to speak with Texas Instruments to  
182       see if they have any recommendations for testing the  
183       performance of this circuit, since my DAC circuit is similar  
184       to one of the TI evaluation boards.  
185           a. I was able to get a nice looking waveform to come  
186       out of the DAC5682Z and the analog circuit, so

May 17, 09 14:42

pcb\_turnon\_notes.txt

Page 4/5

```

187     I suspect to the problem lies with the resolution
188     and sample rate of the signals being sent to the
189     DAC5682Z. I may need to generate the signals with
190     more precision than 16-bits, and dither the LSB
191     bits before/after truncation occurs with a
192     4- to 6-bit PRBS signal.
193     b. Another alternative for signal generation is an
194     8 channel DDS implementation. I'd need to design
195     the DDS in Verilog, and this would take a week or
196     two of design time. With a DDS I would be able
197     to dynamically change frequency and phase without
198     reloading a waveform into either Block RAM or QDR-II SRAM.
199     i. Leveraged a DDS from another design I created into
200     an 8 phase DDS design. The output of the DAC5682Z
201     didn't look much better. There could still be a
202     timing problem with the 16-bit data bus due to the
203     PC Board traces being routed shortest length from
204     the Virtex-5 to the DAC5682Z. Probably need to
205     tweak the fixed delay values in the IODELAY blocks.
206     Measure the alignment from each data bit to the
207     clock bit to determine the approximate setup/hold.
208     Use one of the test patterns that provide alternating
209     1's and 0's.
210 16. Review AD9516 differential voltage settings to optimize resulting
211     common mode voltages on all clock outputs.
212     a. See schematics for estimated common voltages of DAC5682Z,
213     AD9516, and Virtex-5.
214         i. DAC5682Z - Measured at DAC5682Z
215             - Vicm: 0.9V (spec), 0.9V (meas)
216             - Vdiff: 0.5V to 1V (spec), 0.328V (meas)
217                 a. Changed Vodiff on AD9516 from 600mV to 960mV.
218                 b. New Measurements; Vidiff: 580mV
219         ii. DAC5682Z - Measured at AD9516
220             - Vocm: 1.335V (spec), 2.09V (meas)
221             - Vodiff: 600mV (spec), 540mV (meas)
222                 a. Changed Vodiff on AD9516 from 600mV to 960mV.
223                 b. New Measurements; Vodiff: 750mV
224         iii. ADS5463 - Measured at ADS5463
225             - Vicm: 2.4V (spec), 2.41V (meas)
226             - Vdiff: 0.5V to 5V (spec), 600mV (meas)
227         iv. ADS5463 - Measured at AD9516
228             - Vocm: 0.920V (spec), 2.0V (meas)
229             - Vodiff: 960mV (spec), 760mV (meas)
230                 a. The Vocm spec is an estimated value based
231                    on Vodiff.
232     b. Verify that clocks get into Virtex-5 FPGA.
233
234
235 #-----
236 # P C B M O D I F I C A T I O N S :
237 #-----
238 1. Load the following Data Path FPGA Configuration Resistors:
239     - R569; CUST_INIT_B
240     - R568; CUST_CFG_DONE
241     - R566; CUST_PROG_B
242     - R567; CUST_CCLK
243 2. DAC5682Z Channel A/B swap:
244     - Remove R88, R89, R530, and R531.
245     - Solder a wire from pad 1 of R88 to pad 2 of R531.
246     - Solder a wire from pad 1 of R89 to pad 2 of R530.
247
248 #-----

```

May 17, 09 14:42

pcb\_turnon\_notes.txt

Page 5/5

```
249 # P C B A S S E M B L Y   S T A T U S   /   P R O B L E M S :
250 #-----
251
252 SN1.1:
253     1. Load Resistors Listed Above. (Completed)
254     2. C15 package (0508) was standing on its edge, rather
255        than lying flat.
256 SN1.2:
257     1. Load Resistors Listed Above. (Completed)
258 SN1.3:
259     1. Load Resistors Listed Above. (Completed)
260     2. J40 SMA Connector Center Pin cracked solder joint at
261        trace landing.
262         a. Reflowed center pin to make good contact.
263     3. U45 VDD Pin 5 was not soldered down (i.e., floating).
264         a. Temporarily pressed pin down to make contact.
265         b. Re-solder joint to make good connection.
266 SN1.4:
267     1. Load Resistors Listed Above. (Completed)
268     2. Perform DAC5682Z Channel A/B swap as described
269        above. (Completed).
270 SN1.5:
271     1. Load Resistors Listed Above. (Completed)
272
273
274 #-----
275 # P C B F A B R I C A T I O N   P R O B L E M S :
276 #-----
277
278 1. Incorrect decal used for U42.
279     a. Designed interposer board to fix decal.
280
```