Agilent Technologies

10 GHz Phase-Locked YIG Source

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Abstract

I worked on the design of a 10 GHz phase-locked yttrium iron garnet (YIG) source with a selectable output frequency for an Agilent Technologies 13 Gb/s general purpose bit-error-ratio tester (BERT), which is a replacement for the newly released 3 Gb/s BERT. The main tools that were used to test the functionality of the 10 GHz YIG source were an Agilent Technologies 1.5 GHz Infiniium Oscilloscope and a 50 GHz Portable Spectrum Analyzer. The selected operating frequency of the 10 GHz YIG source was approximately produced in the beginning, but soon after the frequency shifted from the desired output. The 10 GHz YIG source was able to operate at frequencies in the range of 3.3 GHz to 11.29 GHz. The 10 GHz YIG source was theoretically supposed to operate at frequencies in the range of 3.2 GHz to 10.0 GHz. The 10 GHz YIG source was successfully built, and changes (called butches) were successfully made to the design. The butches consisted of adding resistor dividers, making new connections between the parts on the PCB, and using different package types for the parts on the PCB.

Introduction:

As the communications industry transitions from second generation (2G) to third generation (3G) technology, data rates increase, resulting in a greater demand for fast and reliable testing equipment. Data rates are increasing so quickly that once a product finally reaches the marketplace, it needs to be redesigned to operate at a faster speed. For example, Agilent Technologies, a leading test equipment manufacturer, only recently released a 3gigabit per second (Gb/s) general purpose bit-error-ratio tester (BERT) that already needs to be redesigned to meet demand. During my internship with Agilent Technologies, I worked on the design of a 10 gigahertz (GHz) phase-locked yttrium iron garnet (YIG) source with my mentor Sam Walker, a hardware design engineer. The 10 GHz YIG source will be used as a clock source on Agilents new13 Gb/s general-purpose BERT. The 13 Gb/s BERT will replace the 3 Gb/s BERT.

Specifications:

The 10 GHz YIG source has a selectable frequency output from 3 GHz to 10 GHz. The source uses a 7.3728 MHz reference oscillator to lock to the desired frequency and is driven by an Agilent Technologies Raven-Lucy 3.3 GHz to 10.2 GHz oscillator. My task was to get the source to select and/or lock to a desired frequency. My objective for this design was to assemble and debug the source, write all of the software for the main parts of the 10 GHz YIG source, and meet the above frequency specifications.

Design and Methodology:

The first step in this design was to test the voltage sources for proper functionality. The correct voltages had to be provided to the appropriate locations. Once this had been achieved, I then had to attach the main parts of the source one by one, and make any necessary modifications to the design. The main parts of the 10 GHz phase-locked YIG source are a PIC16F877 (PIC) 40-pin 8-bit CMOS flash microcontroller, a direct digital modulation Fractional-N frequency synthesizer (Frac-N), and a low-power, dual, 13-bit, voltage-output Digital-to-Analog Converter (DAC).

PIC:

The PIC provides a high-performance RISC CPU, single 5V in-circuit serial programming (ICSP) capability, and universal synchronous asynchronous receiver transmitter (USART) with 9-bit address detection. The PIC operates at a clock speed of 7.3728 MHz. The PIC is the brain of the 10 GHz Phase Locked YIG source; it communicates with the Frac-N and the DAC via one of its input/output (I/O) ports.

The PIC was programmed using an MPLAB assembler and a PICSTART Plus development programmer from Microchip Technology. Both the assembly and C languages were used to set up the receive and transmit terminals, the I/O ports, and the RS-232 communications with a personal computer. The PIC was used to produce the clocks, the data, and the chip selects needed to operate the chips.

The RS-232 port was found to be incorrectly configured as a result of programming the PIC. To track down the problem Microchips in-circuit debugger (ICD) was used to step through the code, watching as the values in the RS-232 ports get updated. The ICD figured out that the serial transmit and serial receive functions were not setting the transmit and receive bits correctly. Once these functions were fixed the PIC was able to communicate via RS-232. A correctly configured RS-232 port is required for the 10 GHz phase-locked YIG source to be user friendly. Using an RS-232 port one would be able to select the desired frequency and the operating voltage of the Frac-N and the DAC, respectively. The PIC would then use these values to compute the binary register values necessary to program the Frac-N and the DAC.

Frac-N:

The Frac-N provides ultra-fine frequency resolution of less than 400 Hz, fast switching speed, and low phase-noise performance. The Frac-N can be used with a reference oscillator up to 50 MHz, and operates at a frequency of up to 6.0 GHz. It uses a 3-wire serial interface which consists of three pins: Clock, Data, and /CS.

Using MATLAB and Microsoft Visual C++, a program was written to convert the desired operating frequency of the 10GHz phase-locked YIG source and the 7.3728 MHz reference oscillator into the proper register values for the Frac-N. The program incorporated the Frac-N register equations, shown in figure 1, and a function that converted the final decimal result into a binary number. The binary number was then programmed into the registers of lengths 9 bits, 8 bits, and 10 bits for the Main Divider, Main Dividend LSB, and the Main Dividend MSB, respectively. The size of the variables and the number of function calls made had to be considered, because this program was to be assembled into a hex file and put into a PIC16F877 microcontroller.

Throughout the building of the 10 GHz YIG source, it was found that the oscillator input was preventing the Frac-N from producing a pulse width modulated square wave. To fix this problem, a 0.1μF capacitor was added to the oscillator input and a 5kΩ resistor was added to the phase detector output. Upon adding the parts, the Frac-N began producing a pulse width modulated square wave with a peak-to-peak voltage of 50mV, rather than the expected 5V. To adjust the output voltage the gain of the main charge pump phase detector was reprogrammed to its maximum value. Upon reprogramming the Frac-N, the output voltage had increased to 300mV, which was still lower than the 5V specification. In addition, a resistor divider was added to increase the gain of the output voltage. Unfortunately, when the resistor divider was added, too much current was being driven through the FM Coil and, consequently, produced incorrect results. The output of the Frac-N was verified by using an Agilent Technologies 50 GHz Portable Spectrum Analyzer and a High Frequency Probe.

Figure 1: Frac-N register equations

The desired division ratio for the Main Synthesizer is given by:

$$\mathbf{N}_{fractional} = \mathbf{F}_{VCO\_main} \ / \ (\mathbf{4 \ x \ F}_{div\_ref} \ )$$

where N fractional must be between 150 and 2150 for the main synthesizer.

The value to be programmed in the Main Divider Register is given by:

$$\mathbf{N}_{reg} = \mathbf{round(N}_{fractional}\mathbf{) \ - \ 32}$$

When in fractional mode, allowed values for N reg are from 6 to 505 inclusive.

The value to be programmed in the Main Dividend Register(s) is given by:

$$\mathbf{dividend = round(divider \ x \ (N}_{fractional} \mathbf{\ - \ N}_{reg} \mathbf{\ - \ 32))}$$

where the **divider** is 262144 in 18-bit mode. Therefore, the dividend is a signed binary value 18 bits long.

DAC:

The DAC features Rail-to-Rail output swing, the ability to update the input and DAC registers independently or simultaneously with a 16-bit serial word, and a 16-bit data-in/data-out shift register. The DAC can produce a 0V to 5V output with a 2.5V reference voltage. It uses a 3-wire serial interface which consists of three pins: Clock, Data, and /CS.

sing the assembly and C programming languages, a program was written to produce the desired output voltage of the DAC. Incorporated in the program were the DAC output voltage equation, shown in figure 2, and a function that converted the final decimal result into a 13-bit binary number. The 13-bit binary number was used for programming the DAC, along with the address bit and two control bits to make up the 16-bit serial input word.

Upon programming the DAC, the output voltage was 0V regardless of the desired output. After researching the properties of the DAC, the clear pin, which automatically set the registers to zero during programming, was discovered. The voltage of the pin was measured while probing the DAC with an Agilent Technologies 1.5 GHz Infiniium Oscilloscope. Once the clear pin was set high the DAC began producing the originally programmed voltages. The output voltage of the DAC was scaled down by an operational-amplifier (op-amp) and then fed into the base of the Darlington power transistor (Main Coil). The Main Coil produced varying frequencies from 3 GHz to 10 GHz depending on the output of the DAC. The Main Coil output was verified by using an Agilent Technologies 50 GHz Portable Spectrum Analyzer. The output frequency of the Main Coil was more unstable than expected in the initial design. Although the output frequency was initially set, it would drift away from the desired output. A possible solution to this problem would be the use of a precision resistor, which would adjust the resistance to the amount of current driven through the Main Coil. To add a precision resistor, the gain of the resistor divider at the negative input of the op-amp has to be lowered to decrease the amount of current driven through the Main Coil. Also, a resistor divider would have to be added to the output of the DAC to scale down the 5V output to about 100mV.

Figure 2: DAC output voltage equation

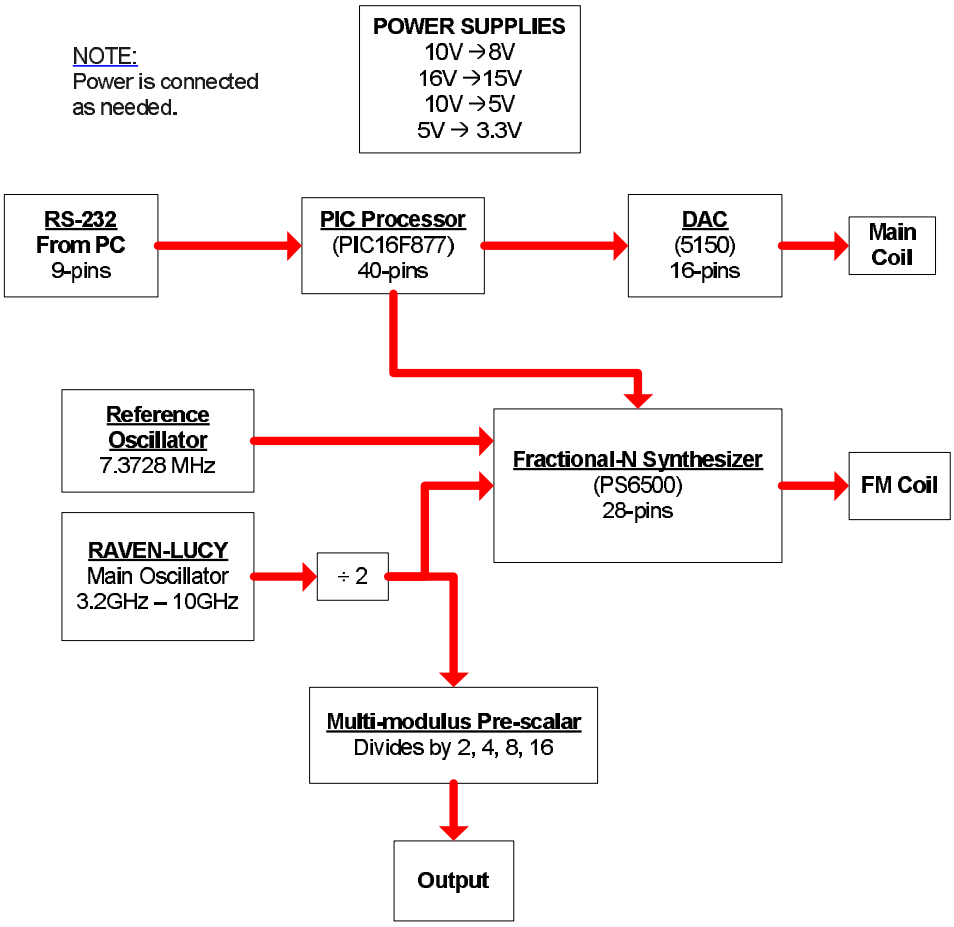
The output voltage is determined using the following equation:

$$\mathbf{VOUT = (VREF \times NB / 8192) \times 2}$$

where NB is the numeric value of the DACs binary input code (0 to 8191) and VREF is the reference voltage, 2.5V.

Block Diagram:

Figure 3: 10 GHz Phase-Locked YIG Source



Implementation:

Overall the design of the sources printed circuit board (PCB) changed four times. Adjustments were made to the voltage sources on the board, the resistor dividers seen at the output of the Main and FM Coils, and the size of the microcontroller pin out on the PCB. Parts were both added to and removed from the PCB. When the PCB was finally ready to be tested the software was assembled and loaded into the PIC, and the source was hooked up to a computer via an RS-232 cable. A simple hyper terminal program was used to communicate with the 10 GHz YIG source and to set up the output of the Frac-N and the DAC. An Agilent Technologies 50 GHz Portable Spectrum Analyzer was used to check the functionality of the board. The spectrum analyzer verified that the source operated effectively except for the instability of the output frequency. However, the output was close to the desired value. Possible solutions to this problem were previously mentioned above when describing the Frac-N and the DAC. The cost of this board varies from the prototype version to the high volume manufactured version. At the prototype level, the PCB costs around $100.00, the PIC costs $20.00, the Frac-N costs $20.00, the DAC costs $23.00, and the Agilent Raven-Lucy Oscillator costs $500.00. Overall, the total prototype cost is $700.00. The manufacturing cost would be higher than the prototype cost, probably around $1000.00.

Functional Testing:

The basic method used to test the functionality of the 10 GHz YIG source is described below.

The microcontroller was programmed with code that produces a known frequency output. While the microcontroller was being programmed, the program pins were probed with an oscilloscope to verify that it was receiving information.

When programming was finished, the output pins were probed and the power supply was cycled to create the wave forms. Trigger on the input to the oscilloscope while cycling the power. If the wave forms were created on the scope, then the output was checked with the program specifications. They should have matched correctly. All of the high to low transitions were checked. If the wave forms were not created, then the microcontroller pins were rechecked verifying correct power and ground connections.

A digital multimeter was used to ohm out all connections from the microcontroller pins to the desired integrated chip (IC). If the connections were all correct, then the microcontroller was reprogrammed and checked again. If a required connection was not made, then a wire was connected from the processors pin to the ICs pin and the microcontroller was reprogrammed and rechecked.

Once all the connections were made and all of the output voltages were correct, the 10 GHz Raven-Lucy oscillator was hooked up to the 10 GHz YIG source. A 50 GHz Spectrum Analyzer was used to check the frequency output. To connect the 10 GHz oscillator a blocking capacitor rated at 26.5 GHz and a 20 dB attenuator rated at 26.5 GHz were used at the input of the 50 GHz Spectrum Analyzer. Then a 26.5 GHz power splitter was used to connect the oscillator to both the 10 GHz YIG source and the Spectrum Analyzer. Once the oscillator was connected the power supplies were turned on. On the Spectrum Analyzer a peak search was performed to find the highest frequency, then that frequency was centered on the screen. The center frequency should correspond to the output voltage of the DAC, where a 1V output corresponds to a low frequency output and a 4V output corresponds to a high frequency output.

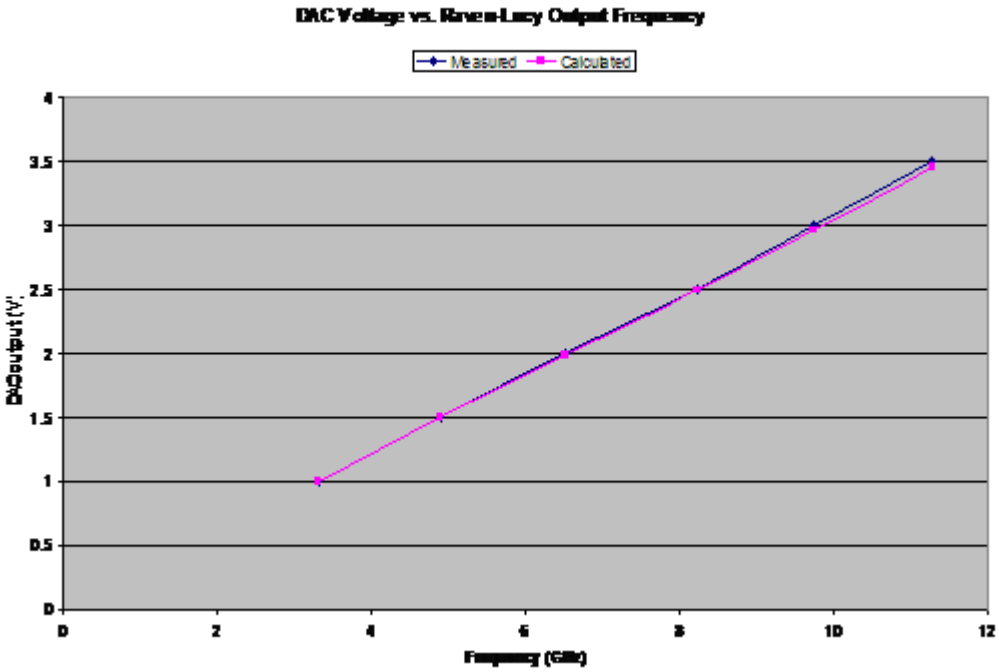
Results:

Looking at table 1 and the figure 4, the output of the 10 GHz phase-locked YIG source is almost linear with respect to the DAC output voltage while running open-loop (i.e., FM Coil is not connected, only Main Coil is in use.). However, if the Frac-N had worked the relation between the output frequency and the DAC voltage would have been approximately linear.

Table 1: DAC output voltage and the corresponding output of the Raven-Lucy Oscillator

Frequency Output	**DAC Output "Calculated"**	**DAC Output "Measured"**
Not enough current to drive the Raven-Lucy Oscillator	0.9V	0.884V
3.306 GHz	1V	0.999V
4.892 GHz	1.5V	1.497V
6.511 GHz	2V	1.978V
8.230 GHz	2.5V	2.495V
9.749 GHz	3V	2.964V
11.290 GHz	3.5V	3.462V

Figure 4: Graph of Calculated vs. Measured voltages vs. Frequency



Discussion:

During the testing of the 10 GHz YIG source, some problems were found with the design that proved to be critical design factors. For example, the oscillator input to the Frac-N needed to be preceded by a 0.1μF capacitor and the phase detector output needed to be followed by a 5kΩ resistor. The missing capacitor and resistor prevented the Frac-N from producing a pulse width modulated square wave.

Upon finishing the 10 GHz phase locked YIG source, its performance was found to be just under the specifications. The selected operating frequency of the 10 GHz YIG source was approximately produced in the beginning, but soon after the frequency shifted from the desired output. The 10 GHz YIG source was able to operate at frequencies in the range of 3.3 GHz to 11.29 GHz. The 10 GHz YIG source was theoretically supposed to operate at frequencies in the range of 3.2 GHz to 10.0 GHz.

The reason for the shifting of the operating frequency was due to the fact that the current through the Main Coil was too large. A possible solution to this problem would be to use a precision resistor, which would adjust the resistance to the amount of current driven through the Main Coil.

Conclusions:

The 10 GHz YIG source was successfully built, and changes (called "butches") were successfully made to the design. The "butches" consisted of adding resistor dividers, making new connections between the parts on the PCB, and using different package types for the parts on the PCB.