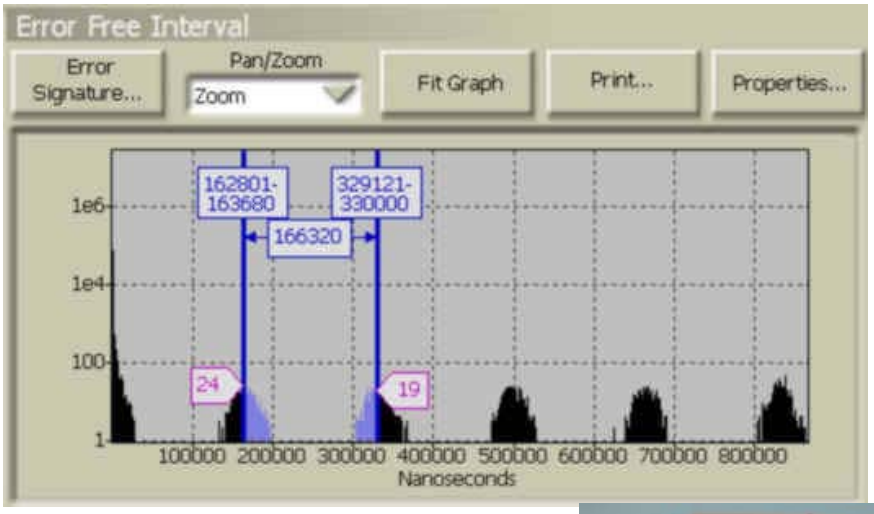
Agilent 86130A BitAlyzer®

Error Analysis Demonstration



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Introduction

Agilent Technologies 86130A BitAlyzer® 3.6 Gb/s error performance analyzer along with error analysis tools, provides you with the unique ability to quickly isolate the causes of errors in your designs. These tools are block analysis, burst lengths, error-free Intervals (EFI), correlation analysis, and pattern sensitivity analysis. To demonstrate error analysis with real world design problems, a transmit and receive module was designed. The custom-built error tester, also known as Jeremy's Error Tester (JET), generates power supply interference (PSI), intermittent parallel bus errors (IPBE), poor signal-to-noise ratio (SNR), and gallium arsenide (GaAs) droop in an optical transceiver design.

Chapter I

86130A BitAlyzer Error Analysis Software Features

Block Analysis

A block is a fixed number of related bits, set by the user and called the data block size. The block can represent the length of an MPEG packet size, 1024, etc. The block analysis describes the error distribution over time that occurs in the group of data contained by the block. The histogram view displays the block error data calculated during error processing. The horizontal axis, block errors (bits), represents the number of errors per block. The vertical axis, occurrences, shows how many block errors have occurred within a given block. This achieves a histogram that represents the quantity of errors from every block of incoming data.[1,2]

Burst Lengths

The burst lengths histogram is useful for understanding the nature of bursts in a channel, and shows the distribution of burst errors of different length. The horizontal axis, burst length (bits), shows the length of burst errors. The vertical axis shows the number of times burst errors with a given length have occurred.[3]

Error-Free Intervals

The EFI tool provides the error free interval length in either bits or time. The horizontal axis, error free interval (bits or nanoseconds), shows the length of an error-free interval. The vertical axis shows how many times an error free interval has occurred. If the errors are all random, then the EFI chart will have a negative slope with no spikes. In this case all error-free intervals have the same probability of occurring. If, however, there are spikes in the chart, this indicates there are systematic errors occurring. Once we know the lengths of the error free intervals, we can calculate the repetition rate of the errors.[4]

Correlation Analysis

Correlation analysis allows you to supply a repeating cycle, or “golden number”. The error position information is correlated with the “golden number”, and the number of channel errors are displayed with respect to position in this repeating cycle. If errors relate to the number 10, then the same bin will fill each time around. This will not necessarily be bin number 10, but the fact that any one bin fills up any more frequently than others demonstrates the relationship exists. An incorrectly chosen golden number will yield a flat histogram. Correlation analysis is a very effective way of hunting down problems in channel hardware.

Pattern Sensitivity Analysis

Pattern sensitivity analysis allows you to view the number of errors that are occurring versus the data pattern to see if certain patterns cause more errors than others. With no pattern sensitivity, all bit positions within the pattern are equally likely of being in error. With pattern sensitivity, certain locations within the pattern will cause more errors than others. In the histogram, the bit positions in the pattern are laid out on the horizontal axis with the first bit in the pattern at the left origin. The amount of errors that occur at each bit position in the sequence are plotted in the vertical axis. The cursor can be positioned over the error position in the histogram to show the error amount, position, and correct bit in the data pattern. At the bottom of the histogram window is the correct pseudo random pattern that is being used to check pattern sensitivity.[5] The pattern sensitivity analysis tool displays the data stream generated by the pattern generator and highlights the bit(s) in error.

References

1. “BA3600 Bit Error Analyzer User Guide”, SyntheSys Research Inc. User Guide BA3600-701, 2000, Pg. 50
2. Agilent Technologies, “BER – What is it telling you?”, Poster 5968-5431E, 2000
3. “BA3600 Bit Error Analyzer User Guide”, SyntheSys Research Inc. User Guide BA3600-701, 2000, Pg. 48
4. “BA3600 Bit Error Analyzer User Guide”, SyntheSys Research Inc. User Guide BA3600-701, 2000, Pg. 49
5. “BA3600 Bit Error Analyzer User Guide”, SyntheSys Research Inc. User Guide BA3600-701, 2000, Pg. 54

Chapter II

BitAlyzer Error Analysis Examples

This section presents the examples demonstrated by the JET. In each example, you see the setup used by error analysis and the corresponding results.

All measurements were made using the following initial BitAlyzer settings:

Setup	Selection	Value
Pattern Select	Pattern	2^n–1 PRBS
	Pattern Size	2^{31}-1
	Error Detector Pattern tracks the Pattern Generator Pattern	Make sure this box is checked to turn on
Pattern Generator	Data Output On	Make sure this box is checked to turn on
	Data Tracking On	Make sure this box is checked to turn on
	Data Inverted	Make sure this box is unchecked to turn off
	Data Termination	+1.3V
	Data Logic Level	LVPECL
	Clock Output On	Make sure this box is checked to turn on
	Clock Tracking On	Make sure this box is checked to turn on
	Clock Termination	+1.3V
	Clock Logic Level	LVPECL
	Bit Rate	1.25 Gb/s, Gigabit Ethernet
	Trigger Output	Clock Divide by 8
	Error Add Setup	Off (Only tool bar single error add available)
Error Detector	BER Threshold	1E-2
	Avg. 0/1 Threshold	Make sure this box is unchecked to turn off
	Data Inverted	Make sure this box is unchecked to turn off
	Clock Inverted Edge	Make sure this box is unchecked to turn off
	Data Termination	+1.3V LVPECL
	Clock Termination	+1.3V LVPECL
	Pattern Sync	Normal, Automatic Sync, Sync Threshold: 1E-3

All measurements were made using the following initial JET settings:

Setup	Selection	Value
JET	Power	On
PSI	Amplitude Adjust	Knob turned completely clockwise
Poor SNR	Fiber Optic Cable	Completely screwed into the FC/PC adapter
From PG	Data In	Connect 1 RF SMA cable to the Data Out connector on BitAlyzer
	Data In Bar	Connect 1 RF SMA cable to the Data Out Bar connector on BitAlyzer
	Clock In	Connect 1 RF SMA cable to the Clock Out connector on BitAlyzer
To ED	Data Out	Connect 1 RF SMA cable to the Data in connector on BitAlyzer
	Data Out Bar	Connect 1 RF SMA cable to a channel on an oscilloscope if available

Power Supply Interference

PSI is designed to demonstrate the capability of the EFI and burst lengths tools of error analysis. Typically, PSI occurs when a low-frequency signal couples onto the power plane of an electronic circuit. In this demonstration it is a fiber-optic transceiver and a serializer/deserializer (SERDES) transceiver IC. The JET introduces errors into the data stream. These errors appear as repetitive peaks separated by 1/f when displayed in the EFI tool, where f equals the frequency of the coupled signal. They appear as bursts related to duration of errors in the burst lengths tool. PSI is generated using either a passive or an active bias tee. The bias tee allows the ac content (or a low-frequency signal) to be combined with the dc content (or a power plane at V_{CC}) to produce an ac+dc signal centered at V_{CC}. By adjusting the amplitude of the low-frequency signal the bit-error rate (BER) will decrease or increase. The BER will be zero when the amplitude of the low-frequency signal has been decreased to roughly dc. For a PRBS pattern, the BER will approach roughly 0.5E0 at the maximum amplitude of the low-frequency signal. As the BER gets increasingly worse, the eye diagram will begin to close.

Measurements were made using the following error analysis setup:

Setup	Selection	Value
EFI	Chart Range	Range: 1 to 500,000
	Use Global Time Base	Make sure this box is checked to turn on
	Log Scale	Make sure this box is checked to turn on
Burst Lengths	Chart Range	Range: 1 to 200
	Use Global Time Base	Make sure this box is unchecked to turn off
	Log Scale	Make sure this box is checked to turn on

Measurements were made using the following JET settings:

Selection	Action
PSI	Push “PSI” button once to turn on
PSI Amplitude Adjustment	Turn knob left until desired BER is achieved

An example of the EFI measurement made by the BitAlyzer is shown below:

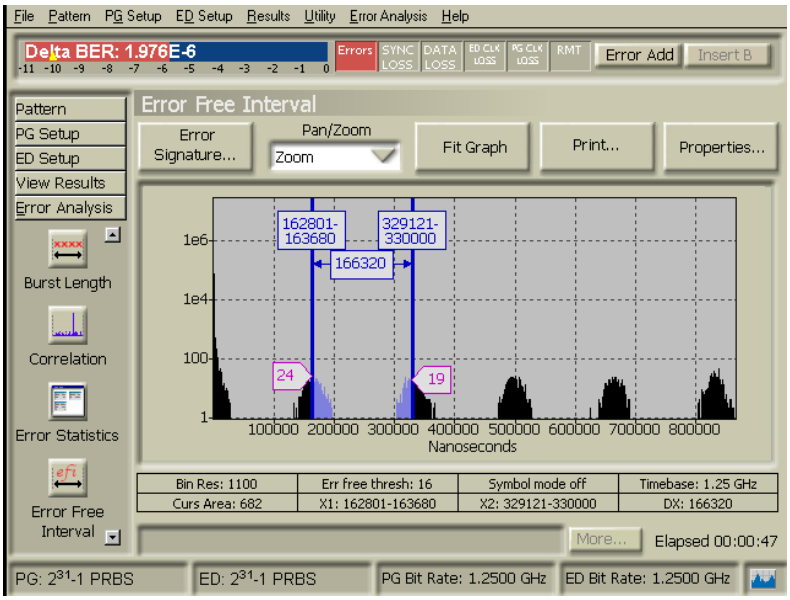

Figure 1. EFI screen capture. Time between bursts is 166320 ns. Frequency of errors is f = 1/t = 6.012 kHz.

An example of the Burst Length measurement made by the BitAlyzer is shown below:

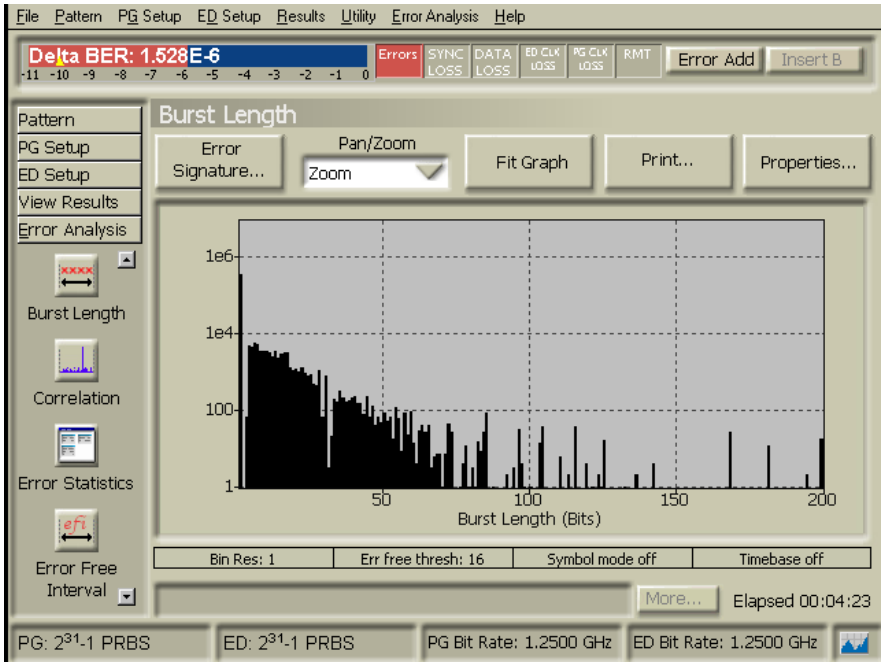

Figure 2. Burst length screen capture. The measurement shows the length of a burst in bits.

An example of the Analyzer control information taken by the BitAlyzer is shown below:

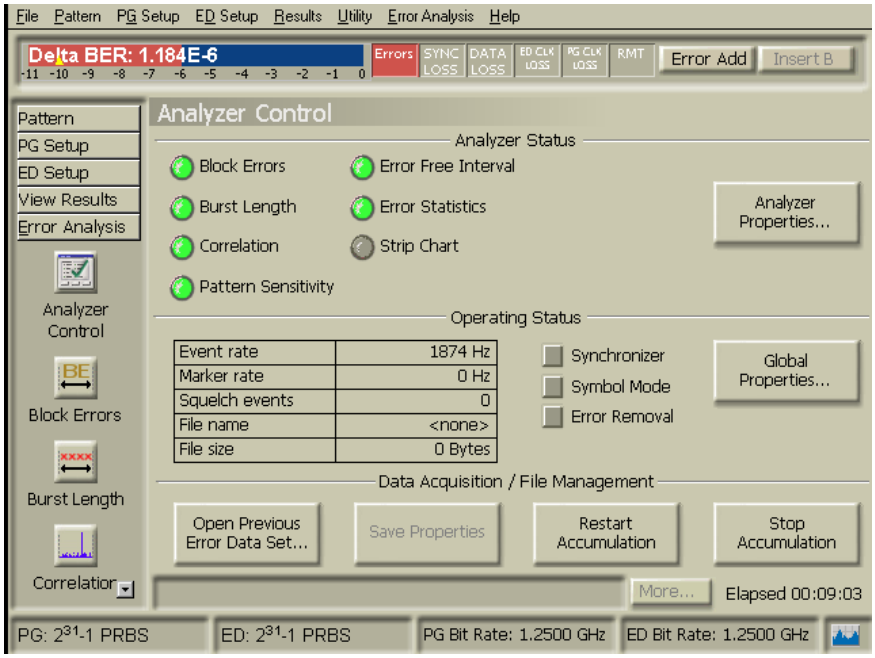

Figure 3. Analyzer control screen capture. Notice the event rate corresponding to PSI measures 1874 Hz. Note: The Event Rate for PSI can vary from 200 Hz to 2 kHz.

Intermittent Parallel Bus Errors

IPBE is designed to demonstrate the capability of correlation analysis, burst lengths, and EFI tools of error analysis. IPBEs can occur when a dry solder joint or unconnected pin exists on the parallel bus of a multiplexer/demultiplexer IC. These errors appear as constant error-free intervals separated by the bus width in the EFI histogram. The burst length histogram displays the errors as one bit errors that accumulate in its first bin. These errors appear as discrete peaks correlated to a "golden number", or bus width, which defines the number of bins present in the correlation tool. IPBE is generated by setting one bit in the 10-bit bus zero every time data is transmitted. The SERDES used in the JET contains a 10-bit bus. When active, the IPBE feature will produce a BER of 0.500E-1.

Measurements were made using the following error analysis setup:

Setup	Selection	Value
Pattern Sync	Sync Threshold	1E-1
Accumulation Setup	Activation Mode	Single
	Measurement Log	No Logging
	Period	Number of Errors: 1000 Errors
Correlation Analysis	Correlation Type	10 bits, Make sure this box is checked to turn on.
	Chart Range	Range: 1 to 10
	Use Global Time Base	Make sure this box is unchecked to turn off
	Log Scale	Make sure this box is checked to turn on
Burst Lengths	Chart Range	Range: 1 to 1000
	Use Global Time Base	Make sure this box is unchecked to turn off
	Log Scale	Make sure this box is checked to turn on
EFI	Chart Range	Range: 1 to 500
	Use Global Time Base	Make sure this box is unchecked to turn off
	Log Scale	Make sure this box is checked to turn on

Measurements were made using the following JET settings:

Selection	Action
Bus Errors	Push "Bus Errors" button once to turn on

An example of the correlation analysis measurement made by the BitAlyzer is shown below:

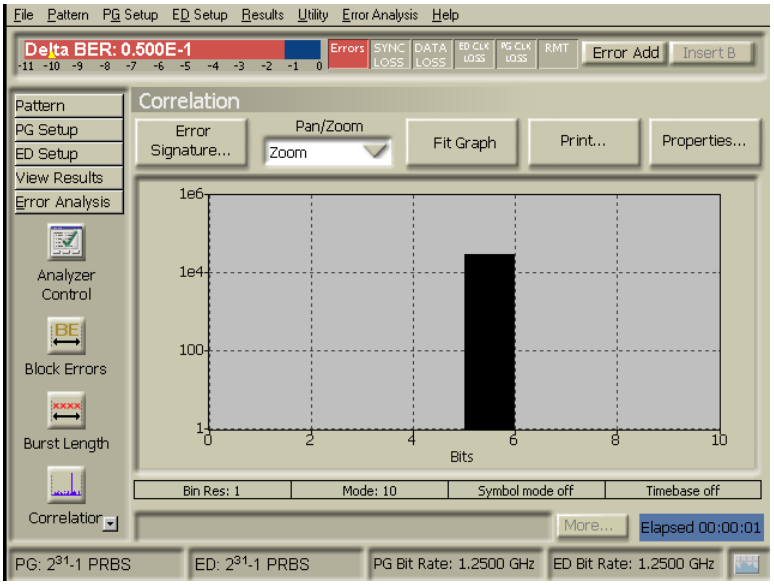

Figure 4. Correlation analysis screen capture. Corresponds to one bit in a 10-bit bus.

An example of the burst length measurement made by the BitAlyzer is shown below:

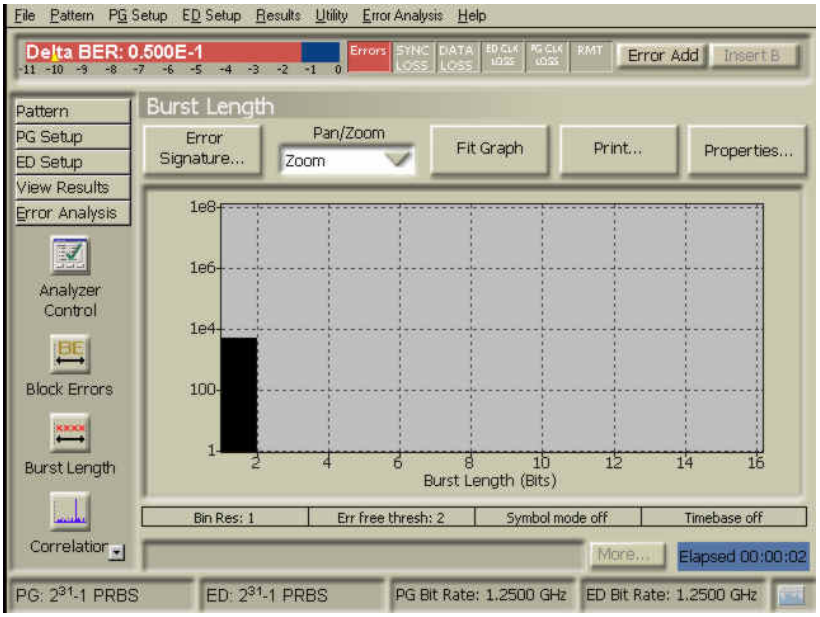

Figure 5. Burst length screen capture. The measurement shows the length of a burst in bits.

An example of the EFI measurement made by the BitAlyzer is shown below:

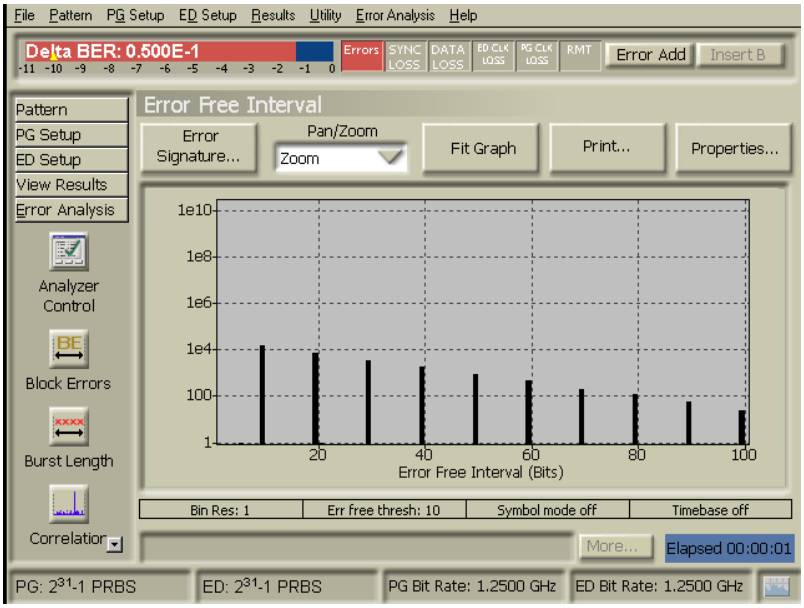

Figure 6. EFI screen capture. The Number of bits between bins is 10, corresponding to the 10-bit bus. If this were truly an intermittent (or random) event, multiple peaks would be observed with a granularity of 10 bit EFI's.

Poor Signal-to-Noise Ratio

Poor SNR is designed to demonstrate the capability of the EFI and burst length tools of error analysis. Typically, poor SNR occurs when an optical data stream is attenuated to a level that causes the eye diagram amplitude to close. The target BER for this error feature is 1.000E-6. This BER produces an error event rate of 200 Hz to 2 kHz, and allows bit errors to accumulate quickly for a demonstration of error analysis. These errors appear as a negative slope in the EFI histogram. They also appear as one bit errors in the first bin of the burst length histogram. Poor SNR is generated by unscrewing the FC/PC connector and gently pulling out the ferrule until the BER changes from 0.000 to approximately 1.000E-6.

Measurements were made using the following error analysis setup:

Setup	Selection	Value
EFI	Chart Range	Range: 1 to 10,000,000
	Use Global Time Base	Make sure this box is checked to turn off
	Log Scale	Make sure this box is checked to turn on
Burst Lengths	Chart Range	Range: 1 to 20
	Use Global Time Base	Make sure this box is checked to turn off
	Log Scale	Make sure this box is checked to turn on

Measurements were made using the following JET settings:

Selection	Action
Poor SNR	Unscrew on end of the fiber-optic cable until desired BER is achieved

To avoid causing the BitAlyzer to squelch, do not completely remove the fiber-optic cable from the FC/PC connector on the JET. Squelching occurs when the bit-error rate tester receives a large amount of bits in error in a short period of time.

An example of the EFI measurement made by the BitAlyzer is shown below:

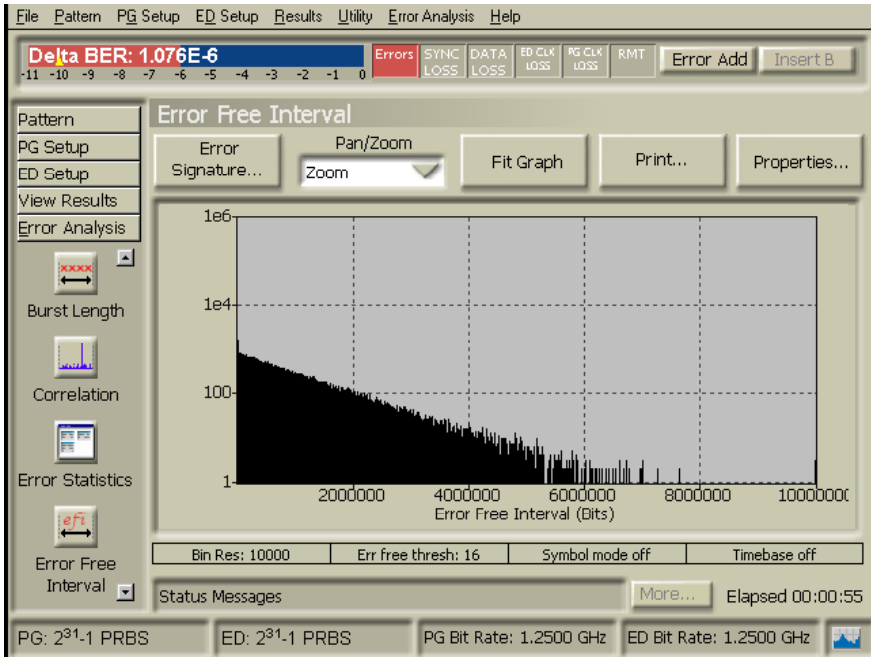

Figure 8. EFI screen capture. These are truly random 1-bit errors if this histogram appears in conjunction with a burst length histogram of length one.

An example of the burst length measurement made by the BitAlyzer is shown below:

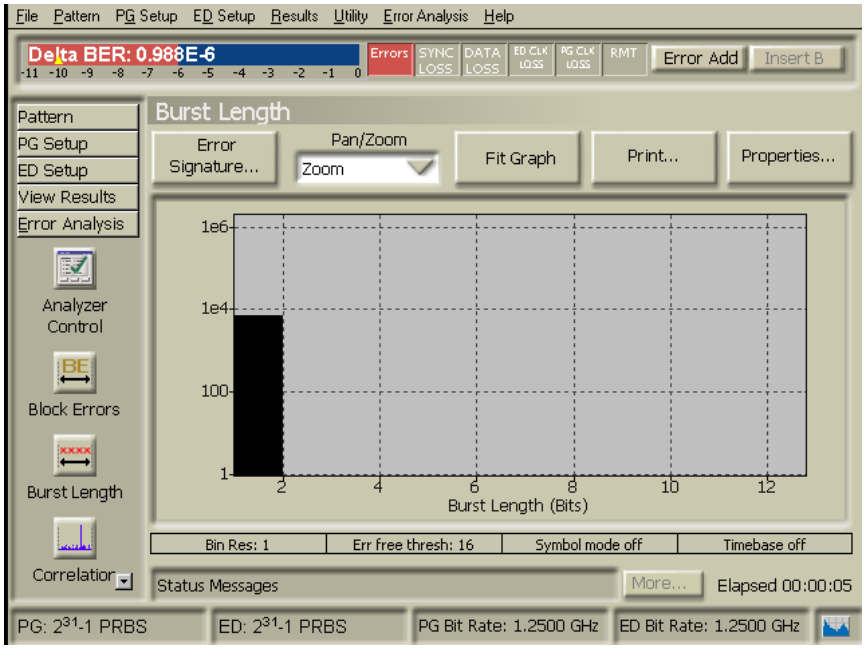

Figure 9. Burst length screen capture. All one bit errors, due to the low probability of bursts of errors from a random event.

An example of the analyzer control information taken by the BitAlyzer is shown below:

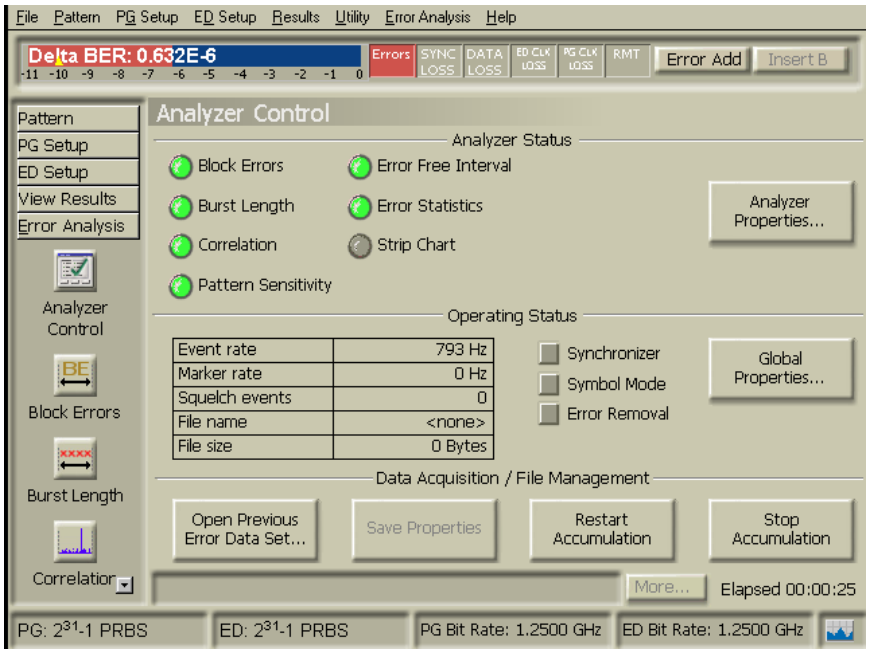

Figure 10. Analyzer control screen capture. Notice the event rate corresponding to poor SNR measures 793 Hz. Note: The event rate for poor SNR can vary from 200 Hz to 2 kHz.

Gallium Arsenide Droop

GaAs droop is designed to demonstrate the capability of the pattern sensitivity analysis tool of error analysis. Typically, GaAs droop occurs when a data stream, consisting of a string of zeros, followed by a one, are driven through a fiber-optic transceiver which uses a GaAs laser driver. In this situation the GaAs laser driver does not have the time to fully acquire the charge to output a completely distinct one. Thus, the error detector on the BitAlyzer may detect a zero rather than a one. Since the fiber-optic transceiver used in the JET design does not contain a discrete laser driver, a simple capacitor was used along with a custom data pattern to simulate the effects of GaAs droop. This design clearly demonstrates the capability of the pattern sensitivity tool. The pattern sensitivity analysis tool displays the data stream generated by the pattern generator and highlights the bit(s) in error.

Measurements were made using the following error analysis setup:

Setup	Selection	Value
Pattern Sensitivity Analysis	Chart Range	Range: 0 to 130
	Use Global Time Base	Make sure this box is unchecked to turn off
	Log Scale	Make sure this box is checked to turn on

Measurements were made using the following JET settings:

Selection	Action
GaAs Droop	Push “GaAs Droop” button once to turn on

An example of the pattern sensitivity analysis measurement made by the BitAlyzer is shown below:

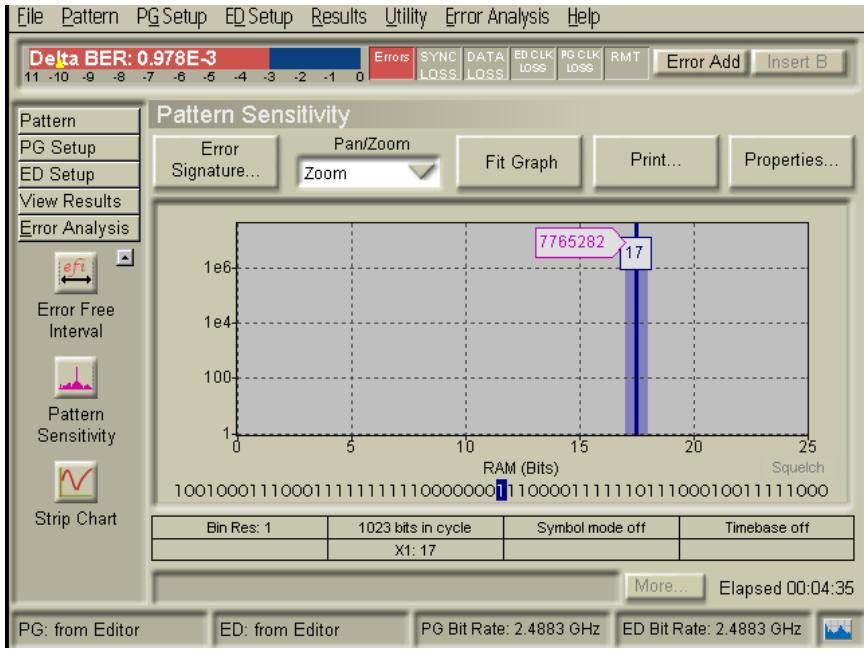

Figure 11. Pattern sensitivity analysis screen capture. Notice the highlighted bit is a one after a long string of zeros.

BitAlyzer is a U.S. registered trademark of SyntheSys Research, Inc.

For more information about Agilent Technologies 86130A BitAlyzer® 3.6 Gb/s error performance analyzer see the following application notes:

1. Guy Foster and Tom Waschura, “Beyond Bit Error Ratio - Gain New Insight from Studying Error Distributions”, Optical Network Interface Design Symposium, September 2000.
2. “An introduction to Error Location Analysis – Are all your errors truly random?” Agilent Technologies Application Note 1550-2, Literature number 5980-0648E. April 2000.
3. “BER – What is it telling you?” Poster, Agilent Technologies Literature Number 5968-9431E, May 2000.

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